LIQUID CRYSTAL DISPLAY DEVICE AND FABRICATING METHOD THEREOF

BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

[0001] The present invention relates to a liquid crystal display, and more particularly to a liquid crystal display device and a fabricating method thereof that are adaptive for improving picture quality.

DESCRIPTION OF THE RELATED ART

[0002] Generally, a liquid crystal display (LCD) controls light transmittance using an electric field to display a picture. To this end, the LCD includes a liquid crystal panel having liquid crystal cells arranged in a matrix type, and a driving circuit for driving the liquid crystal panel. The liquid crystal panel is provided with pixel electrodes for applying an electric field to each liquid crystal cell, and a common electrode. Typically, the pixel electrode is provided on a lower substrate for each liquid crystal cell, whereas the common electrode is integrally formed on the entire surface of an upper substrate. Each of the pixel electrodes is connected to a thin film

transistor (TFT) used as a switching device. The pixel electrode drives the liquid crystal cell, along with the common electrode, in accordance with a data signal applied via the TFT.

[0003] Referring to Fig. 1 and Fig. 2, a lower substrate 1 of a LCD includes a TFT T arranged at an intersection between a data line 4 and a gate line 2, a pixel electrode 22 connected to a drain electrode 10 of the TFT, and a storage capacitor S positioned at an overlapping portion between the pixel electrode 22 and the pre-stage gate line 2.

[0004] The TFT T includes a gate electrode 6 connected to the gate line 2, a source electrode 8 connected to the data line 4, and a drain electrode 10 connected, via a drain contact hole 20, to the pixel electrode 22. Further, the TFT T includes semiconductor layers 14 and 16 for defining a channel between the source electrode 8 and the drain electrode 10 by a gate voltage applied to the gate electrode 6. Such a TFT T responds to a gate signal from the gate line 2 to selectively apply a data signal from the data line 4 to the pixel electrode 22.

[0005] The pixel electrode 22 is positioned at a cell area divided by the data line 4 and the gate line 2 and is made from a transparent conductive material having a high light transmittance. The pixel electrode 22 generates a potential difference from a common transparent electrode (not shown) provided at an upper substrate (not shown) by a data signal applied via the drain contact hole 20. By this potential difference, a liquid crystal positioned between the lower substrate 1 and the upper substrate (not shown) is

rotated due to its dielectric anisotropy. Thus, the liquid crystal allows a light applied, via the pixel electrode 22, from a light source to be transmitted into the upper substrate.

[0006] The storage capacitor S charges a voltage in an application period of a gate high voltage to the pre-stage gate line 2 while discharging the charged voltage in an application period of a data signal to the pixel electrode, to thereby prevent a voltage variation in the pixel electrode 22. The storage capacitor S consists of a gate line 2, and a storage electrode 24 overlapping with the gate line 2 and having a gate insulating film 12 disposed therebetween and being electrically connected, via a storage contact hole 26 defined at a protective film 18, to the pixel electrode 22.

[0007] A method of fabricating the lower substrate 1 of the liquid crystal display having the above-mentioned configuration will now be described.

[0008] First, a gate metal layer is deposited onto the lower substrate 1 and then patterned to form the gate line 2 and the gate electrode 6 as shown in Fig. 3A. An insulating material is entirely deposited onto the lower substrate 1 in such a manner to cover the gate line 2 and the gate electrode 6, thereby forming the gate insulating film 12 as shown in Fig. 3B. First and second semiconductor layers are sequentially deposited onto the gate insulating film 12 and then patterned to form an active layer 14 and an ohmic contact layer 16.

[0009] Subsequently, a data metal layer is deposited onto the gate

insulating film 12 and then patterned to form the storage electrode 24, the source electrode 8 and the drain electrode 10 as shown in Fig. 3C. Thereafter, the ohmic contact layer 16 is etched to expose the active layer 14 in order to define a desired size of channel. A portion of the active layer 14 corresponding to the gate electrode 6 between the source electrode 8 and the drain electrode 10 defines a channel.

[0010] Then, a protective film 18 is formed on the gate insulating film 12 and then patterned to form the drain contact hole 20 and the storage contact hole 26 in such a manner to expose the drain electrode 10 and the storage electrode 24 as shown in Fig. 3D.

[0011] Subsequently, a transparent conductive material is deposited onto the protective layer 18 and then patterned to form the pixel electrode 22, electrically contacting the drain electrode 10 and the storage electrode 24 as shown in Fig. 3E.

[0012] In such a conventional LCD, when a gate signal applied to the gate electrode 6 is turned off and thus fallen, a feed-through voltage δVp corresponding to the difference between the data voltage applied to each of the data line (based on a voltage of the common electrode) and the liquid crystal cell voltage charged in the liquid crystal cell is created as indicated in the following equation:

$$\Delta Vp=\{ (C_{gd}/C_{lc}+C_s+C_{gd})\} (V_{gh}-V_{gl}) \quad (1)$$

wherein ΔVp represents the feed-through voltage; Cgd the parasitic capacitor

of the gate/drain electrode; Cst the storage capacitor; Vgh the gate high voltage; and Vgl the gate low voltage.

[0013] This feed-through voltage ΔVp is created by a parasitic capacitor existing between the gate terminal of the TFT and the liquid crystal cell Clc as can be seen from the above equation (1), and which periodically changes the amount of transmitted light of the liquid crystal cell Clc. As a result, a flicker and a residual image emerges at the picture displayed on the LCD.

[0014] In order to sufficiently restrain such a feed-through voltage ΔVp, it is necessary to enlarge the capacitance of the storage capacitor Cst, but the above-mentioned LCD structure has a limit in enlarging the capacitance of the storage capacitor Cst.

SUMMARY OF THE INVENTION

[0015] Accordingly, it is an object of the present invention to provide a liquid crystal display and a fabricating method wherein the capacitance of the storage capacitor is enlarged to improve picture quality.

[0016] In order to achieve these and other objects of the invention, a liquid crystal display device, according to one aspect of the present invention, is proved which includes at least two storage capacitors disposed between a gate line and a capacitor electrode, the gate line being connected, via a contact hole passing through said at least two storage capacitors, to the capacitor electrode.

[0017] In the liquid crystal display device, the capacitor electrode is

made from a transparent conductive material, which is any one of indium-tin-oxide (ITO), indium-zinc-oxide (IZO) and indium-tin-zinc-oxide (ITZO).

[0018] The liquid crystal display device further includes a gate insulating film provided on a substrate; a storage electrode provided on the gate insulating film; and a protective layer provided between the storage electrode and the capacitor electrode.

[0019] The storage capacitor includes a first storage capacitor provided between the storage electrode and the gate line with the intervening gate insulating film; and a second storage capacitor provided between the storage electrode and the capacitor electrode with the intervening protective layer. The first storage capacitor is connected to the second storage capacitor in parallel. The contact hole is at least two holes spaced to each other at a larger length than the width of the storage electrode. The capacitor electrode has a larger length than the storage electrode.

[0020] The liquid crystal display device further includes a gate electrode connected to the gate line; source and drain electrodes provided on the gate insulating film; and a pixel electrode provided on the protective layer to be electrically connected to the drain electrode. The pixel electrode electrically contacts the storage electrode through said contact hole passing through the protective layer. The gate insulating film has a thickness of about 4000Å and the protective layer has a thickness of about 2000Å.

[0021] A method of fabricating the liquid crystal display device according to another aspect of the present invention includes the steps of

forming a gate line on a substrate; forming a gate insulating film on the substrate; forming a storage electrode on the gate insulating film; forming a protective layer on the gate insulating film; defining at least two contact holes to expose the gate line; and forming a capacitor electrode electrically contacting the gate line on the protective layer. In this method, the capacitor electrode is made from a transparent conductive material, which is any one of indium-tin-oxide (ITO), indium-zinc-oxide (IZO) and indium-tin-zinc-oxide (ITZO).

[0022] The at least two contact holes are spaced to each other at a larger length than a width of the storage electrode. The capacitor electrode has a larger length than the storage electrode.

[0023] The method further includes the steps of forming a gate electrode connected to the gate line on the substrate; forming a semiconductor layer on the gate insulating film; forming source and drain electrodes on the semiconductor layer; and forming a pixel electrode on the protective layer. The pixel electrode electrically contacts the storage electrode through the contact hole passing through the protective layer. The gate insulating film has a thickness of about 4000Å and the protective layer has a thickness of about 2000Å.

[0024] Further scope of applicability of the present invention will become apparent from the detailed description given hereinafter. However, it should be understood that the detailed description and specific examples, while indicating preferred embodiments of the invention, are given by way of

illustration only, since various changes and modifications within the spirit and scope of the invention will become apparent to those skilled in the art from this detailed description.

BRIEF DESCRIPTION OF THE DRAWINGS

[0025] These and other objects of the invention will be apparent from the following detailed description of the embodiments of the present invention with reference to the accompanying drawings, in which:

[0026] Fig. 1 is a plan view showing the structure of a lower substrate of a conventional liquid crystal display;

[0027] Fig. 2 is a sectional view of the lower substrate of the liquid crystal display taken along line A-A' of Fig. 1;

[0028] Fig. 3A to Fig. 3E are sectional views showing a process of fabricating the lower substrate of the liquid crystal display shown in Fig. 2, step by step;

[0029] Fig. 4 is a plan view showing the structure of a lower substrate of a liquid crystal display according to an embodiment of the present invention;

[0030] Fig. 5 is a sectional view of the lower substrate of the liquid crystal display taken along lines B-B' and C-C' of Fig. 4;

[0031] Fig. 6 is a circuit diagram of the first and second capacitors shown in Fig. 4;

[0032] Fig. 7 is a circuit diagram of the gate resistor shown in Fig. 4;

and

[0033] Fig. 8A to Fig. 8E are sectional views showing a process of fabricating the lower substrate of the liquid crystal display shown in Fig. 5 step-by-step.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[0034] Fig. 4 and Fig. 5 are respectively a plan view and a sectional view showing the structure of a lower substrate of a liquid crystal display according to an embodiment of the present invention, which emphasizes the thin film transistor portion and the storage capacitor portion.

[0035] Referring to Fig. 4 and Fig. 5, the lower substrate 31 of the liquid crystal display (LCD) includes a TFT T arranged at an intersection between a data line 34 and a gate line 32, a pixel electrode 52 connected to a drain electrode 40 of the TFT T, and a storage capacitor Cs positioned at an overlapping portion among the pixel electrode 52, a capacitor electrode 58 and the pre-stage gate line 32.

[0036] The TFT T includes a gate electrode 36 connected to the gate line 32, a source electrode 38 connected to the data line 34, and a drain electrode 40 connected, via a drain contact hole 50, to the pixel electrode 52. Further, the TFT T includes semiconductor layers 44 and 46 for defining a channel between the source electrode 38 and the drain electrode 40 by a gate voltage applied to the gate electrode 36. The TFT T responds to a gate signal from the gate line 32 to selectively apply a data signal from the data

line 34 to the pixel electrode 52.

[0037] The pixel electrode 52 is positioned at a cell area divided by the data line 34 and the gate line 32 and is made from a transparent conductive material having a high light transmittance. The pixel electrode 52 generates a potential difference from a common transparent electrode (not shown) provided at an upper substrate (not shown) by a data signal applied via the drain contact hole 50. By this potential difference, a liquid crystal positioned between the lower substrate 1 and the upper substrate (not shown) is rotated due to its dielectric anisotropy. Thus, the liquid crystal allows light applied, via the pixel electrode 52, from a light source to be transmitted into the upper substrate.

[0038] The storage capacitor Cs charges a voltage in an application period of a gate high voltage to the pre-stage gate line 32 while discharging the charged voltage in an application period of a data signal to the pixel electrode, thereby preventing a voltage variation in the pixel electrode 22. The storage capacitor Cs consists of first and second storage capacitors Cst1 and Cst2 connected, in parallel, between a capacitor voltage Vp and a gate voltage Vg as shown in Fig. 6.

[0039] The first storage capacitor Cst1 comprises the gate line 32, and a storage electrode 54 which overlaps with the gate line 32 and having a gate insulating film 42 disposed therebetween. The storage electrode 54 is electrically connected, via a first storage contact hole 56a passing through the protective film 48, to the pixel electrode 52. The second storage capacitor

Cst2 comprises the storage electrode 54, and the capacitor electrode 58 which overlaps with the storage electrode 54 and having the protective film 48 disposed therebetween. The capacitor electrode 58 is electrically connected, via second and third storage contact holes 56b and 56c passing through the protective film 48 and the gate insulating film 42, to the gate line 32.

[0040] The capacitance value of the entire storage capacitor Cs which consists of the first and second storage capacitors Cst1 and Cst2 connected in parallel in this manner is more increased by the capacitance value of the second storage capacitor Cst2 than the prior art as given in the following equation:

$$C_s=C_{st1}+C_{st2} \qquad (2)$$

wherein, Cs represents the entire storage capacitor; Cst1 is the first storage capacitor; and Cst2 is the second storage capacitor.

[0041] Since the second storage capacitor Cst2 is formed with intervening protective layer 48 having a thickness of about 2000Å, it can obtain a larger capacitance value at the same area than the conventional storage capacitor S formed with the intervening gate insulating film 42 having a thickness of about 4000Å.

[0042] In the mean time, a gate resistance is decreased by the capacitor electrode 58 having the same potential as the gate line 32 as seen from the following equation:

$$1/R_g = 1/R_{gl} + 1/R_i \quad (3)$$

wherein Rg represents an entire gate resistance; Rgl is a gate line resistance; and Ri is a capacitor electrode resistance.

[0043] Fig. 8A to Fig. 8E show a process of fabricating the lower substrate 31 of the LCD in Fig. 5 step-by-step, emphasizing the thin film transistor portion and the storage capacitor portion.

[0044] Referring to Fig. 8A, the gate line 32 and the gate electrode 36 are provided on the lower substrate 31 of the LCD.

[0045] The gate line 32 and the gate electrode 36 are formed by depositing aluminum (Al) or copper (Cu) onto the lower substrate 31 by a deposition technique such as sputtering, etc., and then they are patterned.

[0046] Referring to Fig. 8B, an active layer 44 and an ohmic contact layer 46 are formed on a gate insulating film 42.

[0047] The gate insulating film 42 is formed by depositing an insulating material onto the entire lower substrate 31 using the plasma enhanced chemical vapor deposition (PECVD) technique in such a manner as to cover the gate line 32 and the gate electrode 36. The active layer 44 and the ohmic contact layer 46 are formed by disposing the first and second semiconductor materials on the gate insulating film 42 and then patterning them.

[0048] The gate insulating film 42 is made from an insulating material such as silicon nitride (SiN_x) or silicon oxide (SiO_x). The active layer 44 is formed from amorphous silicon which is not doped with an impurity. On the

other hand, the ohmic contact layer 46 is formed from amorphous silicon doped with an n-type or p-type impurity.

[0049] Referring to Fig. 8C, the storage electrode 54, the source electrode 38 and the drain electrode 40 are formed on the gate insulating film 42. The storage electrode 54, the source electrode 38 and the drain electrode 40 are formed by entirely depositing a metal layer using the CVD technique or the sputtering technique and then they are patterned. After the source electrode 38 and the drain electrode 40 are patterned, a portion of the ohmic contact layer 46 corresponding to the gate electrode 36 is also patterned to expose the active layer 44. A portion of the active layer 44 corresponding to the gate electrode 36 between the source electrode 38 and the drain electrode 40 defines a channel. The storage electrode 54, the source electrode 38 and the drain electrode 40 are made from molybdenum (Mo) or chromium (Cr), etc.

[0050] Referring to Fig. 8D, the protective layer 48 is provided on the gate insulating layer 42. The protective layer 48 is formed by depositing an insulating material onto the gate insulating layer 42 and then patterning it in such a manner as to cover the storage electrode 54, the source electrode 38 and the drain electrode 40. The drain contact hole 50 and the first storage contact hole 56a are formed in such a manner as to pass through the protective layer 48 to partially expose the surfaces of the drain electrode 40 and the storage electrode 54. Further, the second and third storage contact holes 56b and 56c are formed in such a manner as to pass through

the protective layer 48 and the gate insulating layer 42 to partially expose the surface of the gate line 32.

[0051] The protective layer 48 is made from an inorganic insulating material such as silicon nitride (SiN_x) or silicon oxide (SiO_x), or an organic insulating material such as an acrylic organic compound, Teflon, BCB (benzocyclobutene), Cytop or PFCB (perfluorocyclobutane).

[0052] Referring to Fig. 8E, the pixel electrode 52 and the capacitor electrode 58 are provided on the protective layer 48. The pixel electrode 52 and the capacitor electrode 58 are formed by depositing a transparent conductive material onto the protective layer 48 and then patterning it.

[0053] The pixel electrode 52 electrically contacts the drain electrode 40 through the drain contact hole 50 and electrically contacts the storage electrode 54 through the first storage contact hole 56a. The capacitor electrode 58 is electrically connected, via the second and third storage contact holes 56b and 56c, to the gate line 32.

[0054] Each of the pixel electrode 52 and the capacitor electrode 58 is made from any one of indium-tin-oxide (ITO), indium-zinc-oxide (IZO) and indium-tin-zinc-oxide (ITZO).

[0055] As described above, according to the present invention, at least two storage capacitors disposed between the gate line and the capacitor electrode making the same potential as the gate line, are provided. Accordingly, a capacitance of the entire storage capacitor is enlarged due to a parallel connection of said at least two storage capacitors, so that a

sustaining characteristic of a voltage applied to the liquid crystal can be improved. Also, flicker and a cross talk are reduced to improve picture quality.

[0056] Although the present invention has been explained by the embodiments shown in the drawings described above, it should be understood to one skilled in the art that the invention is not limited to the embodiments shown, but rather that various changes or modifications thereof are can be made without departing from the spirit and scope of the invention.

[0057] The invention being thus described, it will be obvious that the same may be varied in many ways. Such variations are not to be regarded as a departure from the spirit and scope of the invention, and all such modifications as would be obvious to one skilled in the art are intended to be included within the scope of the following claims.